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10/723,414	11/26/2003	Dustin P. Wood	P16830	2632

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EXAMINER	
VIGUSHIN, JOHN B	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 12/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/723,414	WOOD ET AL.
	Examiner	Art Unit
	John B. Vigushin	2841

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Rejections Based On Prior Art

1. The following references were relied upon for the rejections hereinbelow:

Takahashi et al. (US 6,106,923) Neal et al. (US 5,946,470)

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-5, 7, 9-14 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Takahashi et al.

As to Claim 1, Takahashi et al. discloses, in Figs. 6 and 7: a metal layer 12; a first dielectric layer 11 in contact with a first face of the metal layer 12 and a second dielectric layer 13 in contact with a second face of the metal layer 12, the second face being opposite to the first face (col.3: 36-43); wherein the metal layer 12 is a substantially continuous sheet having slots 44 formed therein to allow the first and second dielectric layers 11 and 13 to adhere to each other by way of the slots 44 (col.6: 7-10; col.4: 29-33 implies that there is a sinking of dielectric material 13 into the aperture and into inherently adherent contact with dielectric material 11 that accounts for the "small depressions" formed over layer 13 in the annular aperture embodiment of Fig. 2, which is also shown to occur in the slot embodiment of Fig. 7, wherein the

dielectric material 13 sinks into the slots 44 and into inherently adherent contact with dielectric material 11).

As to Claims 2 and 12, Takahashi et al. further discloses each of the slots 44 has a length:width ratio of at least 5:1 (col.6: 10-14).

As to Claims 3 and 13, Takahashi et al. further discloses the length:width ratio of each slot 44 is at least 10:1 (col.6: 22-24).

As to Claim 4, Takahashi et al. further discloses the slots 44 are arrayed substantially in a rectangular pattern (Fig. 6; col.6: 16-17).

As to Claims 5 and 14, Takahashi et al. further discloses the slots 44 are arrayed substantially in a face-centered rectangular pattern (col.6: 16-17; in Fig. 6, it is disclosed that there is a slot located in the symmetric center of the rectangular pattern of slots; hence, the rectangular pattern of slots is face-centered).

As to Claims 7 and 16, Takahashi et al. further discloses, in the embodiment of Fig. 8 and col.7: 38-41, a first one of the slots has an orientation that is at an angle relative to an orientation of a second one of the slots (e.g., the slots 44' in the center radial pattern, the middle radial pattern and the outermost radial pattern are at an angle relative to one another).

As to Claim 9, Takahashi et al. further discloses the metal layer 12 operates as a ground plane (col.3: 33-36).

As to Claim 10, Takahashi et al. further discloses the metal layer 12 operates as a power plane (col.3: 33-36).

As to Claim 11, Takahashi et al. discloses, in Figs. 6 and 7: forming a metal layer 12 on a first dielectric layer 11, forming a second dielectric layer 13 on the metal layer 12 (col.3: 36-43); the metal layer 12 being patterned as a substantially continuous sheet having slots 44 formed therein to allow for the first and second dielectric layers 11 and 13 to adhere to each other by way of the slots 44 (col.6: 7-10; col.4: 29-33 implies that there is a sinking of dielectric material 13 into the aperture and into inherently adherent contact with dielectric material 11 that accounts for the "small depressions" formed over layer 13 in the annular aperture embodiment of Fig. 2, which is also shown to occur in the slot embodiment of Fig. 7, wherein the dielectric material 13 sinks into the slots 44 and into inherently adherent contact with dielectric material 11).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 6, 8, 15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al.

A) As to Claims 6 and 15:

I. Takahashi et al. discloses the rectangular cell shown in Fig. 6 has an slots with a preferred slot length of at least 10 times the slot width, for example 15 times the slot width (col.6: 22-28) [Takahashi et al. also teaches other length:width slot ratios (col.6: 10-14)]. Using the preferred slot length range of at least 10 times the slot width, the aspect ratio--[horizontal] length L x [vertical] width W--of the rectangular cell in Fig. 6) the rectangular cell shown in Fig. 6 has the following aspect ratios for the given slot width Ws of 10 μm:

a) For a preferred (slot length Ls):(slot width Ws) = 15:1, then slot length Ls = 150 μm. It follows from Fig. 6 and col.6: 22-28 that cell length L = 5 x 150 μm + 4 x 200 μm = 1550 μm; and cell width W = 4 x 200 μm = 800 μm. Therefore, **the aspect ratio L:W = 1550 μm : 800 μm = 1.94: 1**.

b) For a preferred (slot length Ls):(slot width Ws) = 10:1, then Ls = 100 μm. It follows that cell length L = 5 x 100 μm + 4 x 200 μm = 1300 μm; and cell width W = 4 x 200 μm = 800 μm. Therefore, **the aspect ratio L:W = 1300 μm : 800 μm = 1.62 : 1**.

c) Since Takahashi et al. discloses the slot ratio Ls:Ws to be *at least* 10:1, then for an application requiring the slot ratio 12:1, with Ws = 10 μm, then Ls =

120 μm. It follows that cell length L = 5 x 120 μm + 4 x 200 μm = 1400 μm; and cell width W = 4 x 200 μm = 800 μm. Therefore, **the aspect ratio L:W = 1400 μm : 800 μm = 1.75 : 1**.

II. All the above disclosed possible aspect ratios are determined by design factors, as taught by Takahashi et al., and aspect ratios 1.94 : 1 and 1.62 : 1 may reasonably be considered "substantially" 1.73 : 1, as required by Applicant's claim, given the disclosure of Takahashi et al. Most certainly, the aspect ratio 1.75 : 1 is "substantially" 1.73 : 1, as required by Applicant's claim. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the slot ratio Ls:Ws to 12:1 in order to meet the particular design requirements of an application using the multilayer circuit board structure disclosed by Takahashi et al. Furthermore, given the disclosure of the Fig. 6 embodiment of Takahashi et al. in col.6: 7-28, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the slot ratio Ls:Ws to 12:1 in the Fig. 6 embodiment of Takahashi et al. (thereby effectively rendering the rectangular cell aspect ratio L:W = substantially 1.73 : 1), since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

B) As to Claims 8 and 17:

Takahashi et al. discloses a slot width of 10 μm in one embodiment (Fig. 6; col.6: 22-28) and, for good electrical performance (i.e., integrity of controlled impedance) at 200 MHz and above, a recommended maximum slot width of 20 μm (col.7: 45-53), with

the maximum slot width (Wmax) computed on the basis of the thicknesses of dielectric layer 13 and metal layer 12 according to the formula Wmax = 10 μm x (dielectric layer 13 thickness ÷ conductive layer 12 thickness). See col.4: 46-61. Since the invention disclosed by Takahashi et al. is conceived for enabling effective venting of gasses trapped in underlying dielectric layers in multilayer circuit boards, and since such circuit boards are used in low as well as high frequency applications, then determining the parameters of dielectric and metal layer thicknesses, and slot widths for a particular application depend *at least* on the operational range of frequency of an electronic application and on the type of polyimides and conductive metals used for the multilayer board, said resulting slot widths being well within the range of thicknesses and widths determined by the above-cited Wmax formula for that particular application. The operational frequency range of greater than 200 MHz cited by Takahashi et al. in col.7: 45-53 is only an exemplary electronic application of the disclosed multilayer circuit board. Therefore, one of ordinary skill in the art at the time the invention was made would have no difficulty in arriving at an optimal slot width of 50 μm since the conditions for arriving at such a slot width are already disclosed by Takahashi et al. in the slot width formula and discussion in col.4: 46-61, wherein the combination of dielectric and conductive metal materials and operational frequency requirements for meeting the conditions of a particular electronic application would result in an optimal slot width of substantially 50 μm for effective degassing performance without adversely affecting the controlled impedance of the signal lines in the multilayer board. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to

design the multilayer circuit board of Takahashi et al. such that each of the slots 44 has a width dimension of substantially 50 μm for meeting the electronic and material requirements of an application and, further, because it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art, which would certainly be the case in modifying Takahashi et al., given the disclosure of Takahashi et al., as described above. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

7. Claims 18-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. in view of Neal et al.

A) As to Claim 18:

I. Takahashi et al. discloses, in Figs. 6 and 7, a substrate comprising: a metal layer 12; a first dielectric layer 11 in contact with a first face of the metal layer 12 and a second dielectric layer 13 in contact with a second face of the metal layer 12, the second face being opposite to the first face (col.3: 36-43); wherein the metal layer 12 is a substantially continuous sheet having slots 44 formed therein to allow the first and second dielectric layers 11 and 13 to adhere to each other by way of the slots 44 (col.6: 7-10; col.4: 29-33 implies that there is a sinking of dielectric material 13 into the aperture and into inherently adherent contact with dielectric material 11 that accounts for the "small depressions" formed over layer 13 in the annular aperture embodiment of Fig. 2, which is also shown to occur in the slot embodiment of Fig. 7, wherein the dielectric material 13 sinks into the slots 44 and into inherently adherent contact with dielectric material 11).

II. Takahashi et al. does not disclose a die mounted on the substrate and comprising an integrated circuit, and a chipset in communication with the integrated circuit via the substrate.

III. Neal et al. discloses a die 105 mounted on the substrate 110 (motherboard) and comprising an integrated circuit 140, and a chipset 400 in communication with the integrated circuit 140 via the motherboard substrate for performing an electronic function that includes computer processing as required by an application (col.3: 53-55; col.5: 59-col.6: 14; col.6: 30-36).

IV. Since both Takahashi et al. discloses a circuit board structure for use in electronic packages for electronic system applications, wherein the circuit board performance reliability is ensured by the effective degassing and controlled impedance enabled by said circuit board structure (Abstract), and the circuit board package of Neal et al. includes circuit components for performing a particular electronic system function requiring computer processing for a system application, then the mounting of such circuit components, for performing an electronic system function requiring computer processing, onto the performance-enhanced circuit board of Takahashi et al. would have been readily recognized in the pertinent art of Takahashi et al. as resulting in an electronic package with high performance reliability.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Takahashi et al. such that the die comprising the processing integrating circuit of Neal et al. is mounted onto the circuit board of Takahashi et al., and the chipset of Neal et al. is in communication with the integrated

circuit via the performance-enhanced circuit board substrate of Takahashi et al. in order to make use of the circuit board of Takahashi et al. in an electronic package for performing computer processing of signals required by the system application, as taught by Neal et al., and with a high degree of reliability due to the performance-enhanced circuit board structure of Takahashi et al.

B) As to Claim 19, Takahashi et al. further discloses each of the slots 44 has a length:width ratio of at least 5:1 (col.6: 10-14).

C) As to Claim 20, Takahashi et al. further discloses the length:width ratio of each slot 44 is at least 10:1 (col.6: 22-24).

D) As to Claim 21, Takahashi et al. further discloses the slots 44 are arrayed substantially in a rectangular pattern (Fig. 6; col.6: 16-17).

E) As to Claim 22, Takahashi et al. further discloses the slots 44 are arrayed substantially in a face-centered rectangular pattern (col.6: 16-17; in Fig. 6, it is disclosed that there is a slot located in the symmetric center of the rectangular pattern of slots; hence, the rectangular pattern of slots is face-centered).

F) As to Claim 23:

I. Takahashi et al. discloses the rectangular cell shown in Fig. 6 has an slots with a preferred slot length of at least 10 times the slot width, for example 15 times the slot width (col.6: 22-28) [Takahashi et al. also teaches other length:width slot ratios (col.6: 10-14)]. Using the preferred slot length range of at least 10 times the slot width, the aspect ratio--[horizontal] length L x [vertical] width W--of the rectangular cell in Fig. 6)

the rectangular cell shown in Fig. 6 has the following aspect ratios for the given slot width Ws of 10 μm:

a) For a preferred (slot length Ls):(slot width Ws) = 15:1, then slot length Ls = 150 μm. It follows from Fig. 6 and col.6: 22-28 that cell length L = 5 x 150 μm + 4 x 200 μm = 1550 μm; and cell width W = 4 x 200 μm = 800 μm. Therefore, **the aspect ratio L:W = 1550 μm : 800 μm = 1.94: 1**.

b) For a preferred (slot length Ls):(slot width Ws) = 10:1, then Ls = 100 μm. It follows that cell length L = 5 x 100 μm + 4 x 200 μm = 1300 μm; and cell width W = 4 x 200 μm = 800 μm. Therefore, **the aspect ratio L:W = 1300 μm : 800 μm = 1.62 : 1**.

c) Since Takahashi et al. discloses the slot ratio Ls:Ws to be *at least* 10:1 (col.6: 22-24), then for an application requiring the slot ratio 12:1, with Ws = 10 μm, then Ls = 120 μm. It follows that cell length L = 5 x 120 μm + 4 x 200 μm = 1400 μm; and cell width W = 4 x 200 μm = 800 μm. Therefore, **the aspect ratio L:W = 1400 μm : 800 μm = 1.75 : 1**.

II. All the above disclosed possible aspect ratios are determined by design factors, as taught by Takahashi et al., and aspect ratios 1.94 : 1 and 1.62 : 1 may reasonably be considered "substantially" 1.73 : 1, as required by Applicant's claim, given the disclosure of Takahashi et al. Most certainly, the aspect ratio 1.75 : 1 is "substantially" 1.73 : 1, as required by Applicant's claim. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the slot ratio Ls:Ws to 12:1 in order to meet the particular design requirements of an

application using the multilayer circuit board structure disclosed by Takahashi et al. Furthermore, given the disclosure of the Fig. 6 embodiment of Takahashi et al. in col.6: 7-28, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the slot ratio Ls:Ws to 12:1 in the Fig. 6 embodiment of Takahashi et al. (thereby effectively rendering the rectangular cell aspect ratio L:W = substantially 1.73 : 1), since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

G) As to Claim 24, Takahashi et al. further discloses, in the embodiment of Fig. 8 and col.7: 38-41, a first one of the slots has an orientation that is at an angle relative to an orientation of a second one of the slots (e.g., the slots 44' in the center radial pattern, the middle radial pattern and the outermost radial pattern are at an angle relative to one another).

H) As to Claim 25:

Takahashi et al. discloses a slot width of 10 μm in one embodiment (Fig. 6; col.6: 22-28) and, for good electrical performance (i.e., integrity of controlled impedance) at 200 MHz and above, a recommended maximum slot width of 20 μm (col.7: 45-53), with the maximum slot width (Wmax) computed on the basis of the thicknesses of dielectric layer 13 and metal layer 12 according to the formula Wmax = 10 μm x (dielectric layer 13 thickness ÷ conductive layer 12 thickness). See col.4: 46-61. Since the invention disclosed by Takahashi et al. is conceived for enabling effective venting of gasses trapped in underlying dielectric layers in multilayer circuit boards, and since such circuit

boards are used in low as well as high frequency applications, then determining the parameters of dielectric and metal layer thicknesses, and slot widths for a particular application depend *at least* on the operational range of frequency of an electronic application and on the type of polyimides and conductive metals used for the multilayer board, said resulting slot widths being well within the range of thicknesses and widths determined by the above-cited Wmax formula for that particular application. The operational frequency range of greater than 200 MHz cited by Takahashi et al. in col.7: 45-53 is only an exemplary electronic application of the disclosed multilayer circuit board. Therefore, one of ordinary skill in the art at the time the invention was made would have no difficulty in arriving at an optimal slot width of 50 μm since the conditions for arriving at such a slot width are already disclosed by Takahashi et al. in the slot width formula and discussion in col.4: 46-61, wherein the combination of dielectric and conductive metal materials and operational frequency requirements for meeting the conditions of a particular electronic application would result in an optimal slot width of substantially 50 μm for effective degassing performance without adversely affecting the controlled impedance of the signal lines in the multilayer board. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to design the multilayer circuit board of Takahashi et al. such that each of the slots 44 has a width dimension of substantially 50 μm for meeting the electronic and material requirements of an application and, further, because it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art, which would certainly be the case in modifying Takahashi et al., given the disclosure of

Takahashi et al., as described above. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

I) As to Claim 26, Takahashi et al. further discloses the metal layer 12 operates as a ground plane (col.3: 33-36).

J) As to Claim 27, Takahashi et al. further discloses the metal layer 12 operates as a power plane (col.3: 33-36).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Klimek et al. (US 4,250,616) discloses ground or power layers having slots that allow the first and second dielectric layers on either side of the ground/power layer to adhere to each other by way of the slots (Figs. 3, 4, 5, 7 and 8; col.3: 7-11; col.4: 31-35 and 59-61; col.6: 17-20 and 42-46; col.6: 63-col.7: 6; col.8: 38-52).

b) Broaddus et al. (US 4,916,260) discloses a metal layer 15 having slots 17 to allow first and second dielectric sheets 21 and 23 to adhere to each other by way of the slots (Figs. 4, 5, 6 and 7; col.5: 1- 4, 33-36, 34-51; col.5: 64-col.6: 4).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
December 02, 2005